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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/301,284 04/28/99 TAKAYAMA

S NAK1-BG86

EXAMINER

TM02/0807

PRICE GESS & UBELL
2100 S E MAIN STREET
SUITE 250
IRVINE CA 92614

VD, T

ART UNIT

PAPER NUMBER

2122
DATE MAILED:

08/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/301,284

Applicant(s)

TAKAYAMA ET AL.

Examiner

Ted T. Vo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04/28/99 and election 6/11/2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 12-48 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 April 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. This action is in response to the communication filed on 6/11/2001.

Applicant's election without traverse of Group I, claims 1-11 in Paper No. 8 is acknowledged. The claims 1-11 will be examining under this action. Since Applicant does not indicate a cancellation of non-elected claims, claims 1-48 are pending in the application. Since applicant elects group I without traverse, cancellation of claims 12-24 is required.

Drawings

2. Figure 35A and figure 35B are objected to by examiner. A boundary between these two figures is unclear. Correction is required.

Information Disclosure Statement

3. The content of information disclosure statement filed 8/13/1999 is not considered by examiner because it is not matched with its submission. The content is indicated as the full reference but the submission is an English abstract. It would be indicating with quote "abstract" in the content or providing with full English version. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 10-11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

n is an arbitrary integer represents the length of a processing packet. n is undetermined and might varied. Claims 10-11 claim a feature in which the specification does not determine or teach how to obtain the number 'n'.

Since shift register based on a determined number while n is undetermined, it must provide logic to detect a length of instruction packet for initiating counter shift. Specification does not teach how to detect this number. Therefore it fails to enable for making and using based on the limitations of claims 10-11.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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7. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Christie et al., US Patent No. 5,559,975.

As per claim 1:

-Regarding claim limitations:

"A processor for reading instructions from a memory according to a program counter, the memory storing instructions in one-byte units, and for executing the read instructions, the program counter including a first program counter and a second program counter, the first program counter indicating a storage position of a processing packet in the memory, the processing packet being composed of an integer number of the one-byte units"

Christie's reference teaches the claim limitations by using a counter which includes a 'less significant program counter portion' to position to a potential next decode program counter value which corresponds to a RISC instruction set (see column 18, lines 4-23)

-Regarding claim limitations:

"the second program counter indicating a position of processing target instruction in the processing packet, the processing target instruction being an operation to be executed by the processor",

Christie's reference teaches the claim limitations by using a 'more significant program counter portion' included with an incrementor to receive a present the program counter value and to increment to the next instruction (see column 18, lines 24-38).

As per claim 2:

-Regarding claim limitations of claim 2, Christie's reference teaches the claim limitations by using the incrementor in association with the 'more significant program counter portion' (see column 18, lines 24-38); and updating the values of the 'less significant program counter portion' by using the carry bits from each adder to carry selector 334 of more significant program counter (see column 10, lines 60-65).

As per claim 3:

-Regarding claim limitations of claim 3, claim 3 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a

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microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 4:

-Regarding claim limitations of claim 4, claim 4 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 5:

-Regarding claim limitations of claim 5, claim 5 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 6:

-Regarding claim limitations of claim 6, claim 6 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 7:

-Regarding claim limitations of claim 7, claim 7 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

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As per claim 8:

-Regarding claim limitations of claim 8, claim 8 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 9:

-Regarding claim limitations of claim 9, claim 9 inherits from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 10:

-Regarding claim limitations of claim 10, functionality claim 10 inherits from a partition of each instruction set.

As per claim 11:

-Regarding claim limitations of claim 11, functionality claim 11 inherits from stored registers used very common in a microprocessor.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoshida, US Patent No. 5,218,711.

Nanba, US Patent No. 5,819,081.

Sibigtroth et al., US Patent No. 5,475,822.

Bharadhwaj, US Patent No. 6,088,779.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark R. Powell, can be reached on (703) 305-9703. The fax phone number for this Group is (703) 308-1396.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TTV
August 3, 2001


MARK R. POWELL
SUPERVISORY PATENT EXAMINER
GROUP 2700